2003 IRPS

High Performance Logic Technology and Reliability Challenges

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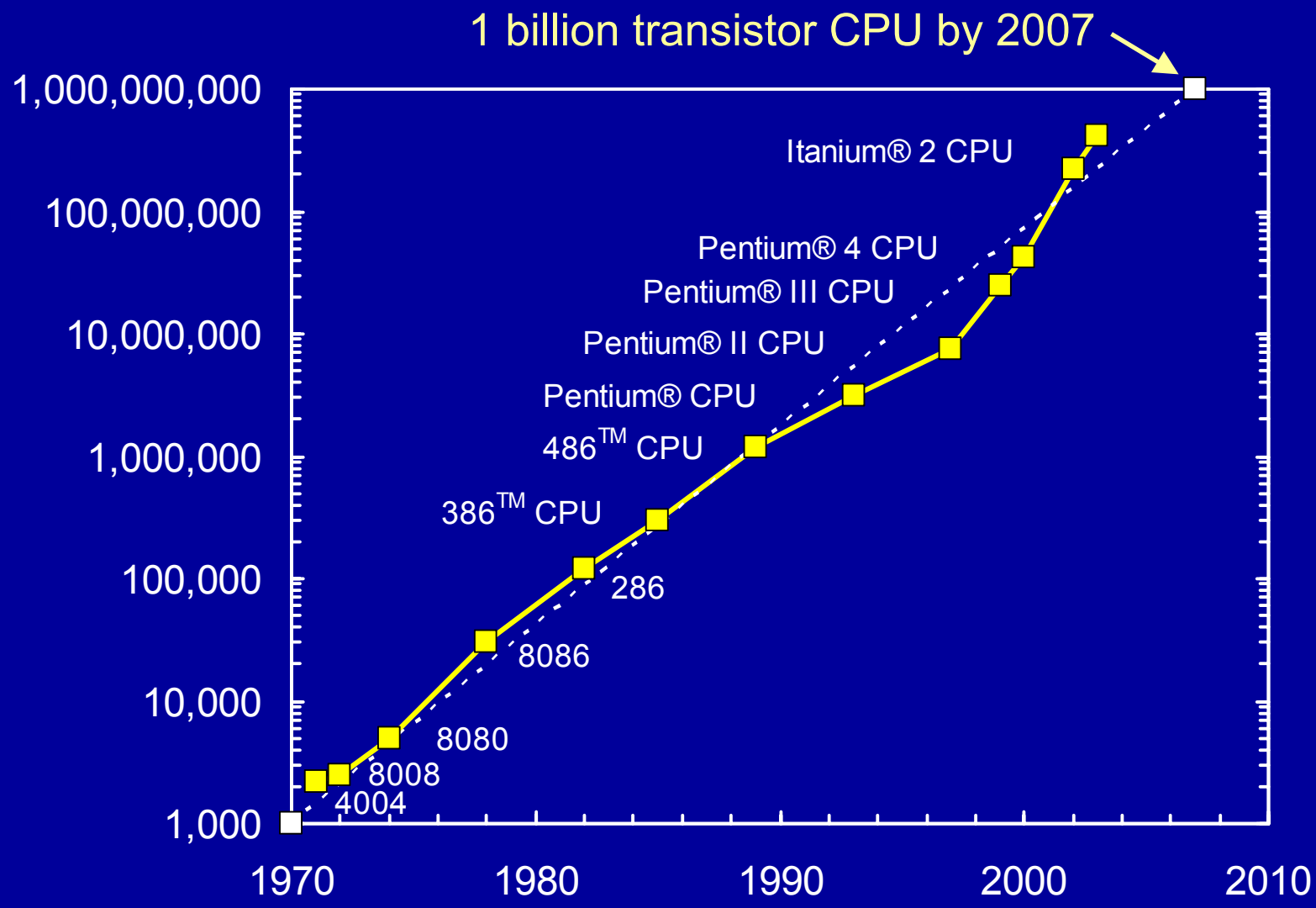
April 1, 2003

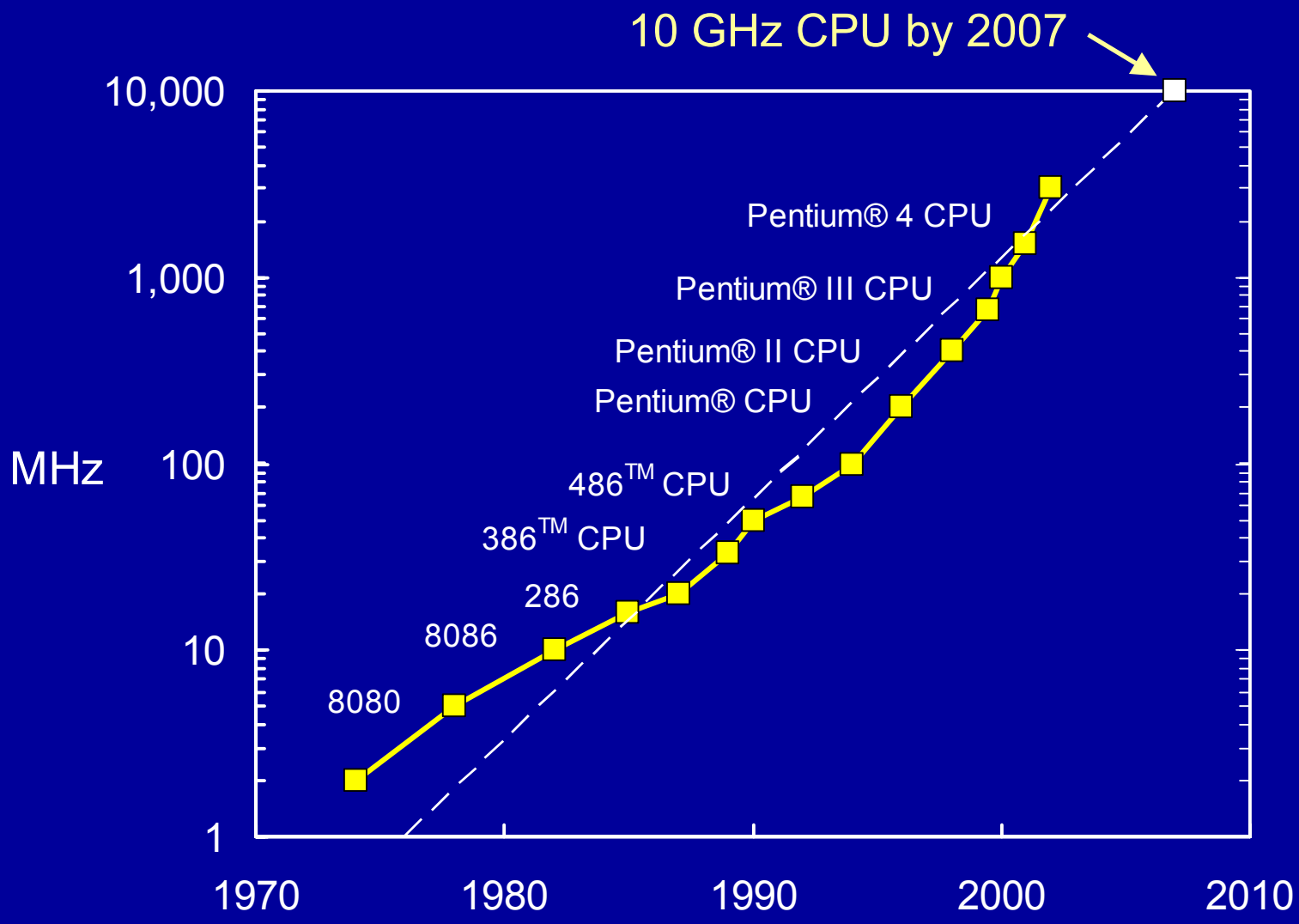
Outline

- Logic Technology Evolution
- 90 nm Logic Technology
- Future Scaling Challenges

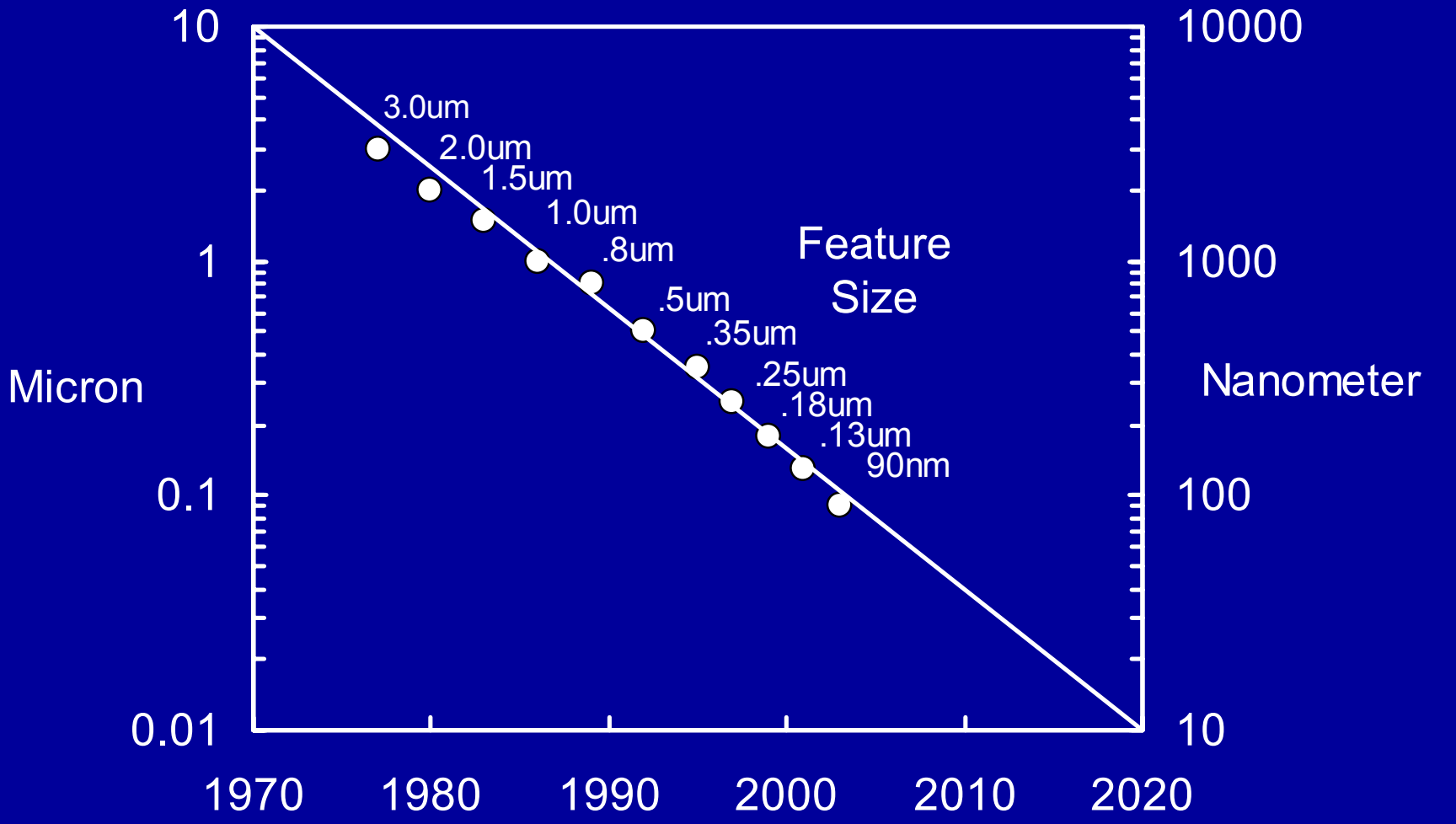
CPU Transistor Count Trend



CPU MHz Trend



Feature Size Trend



New technology generation introduced every 2 years

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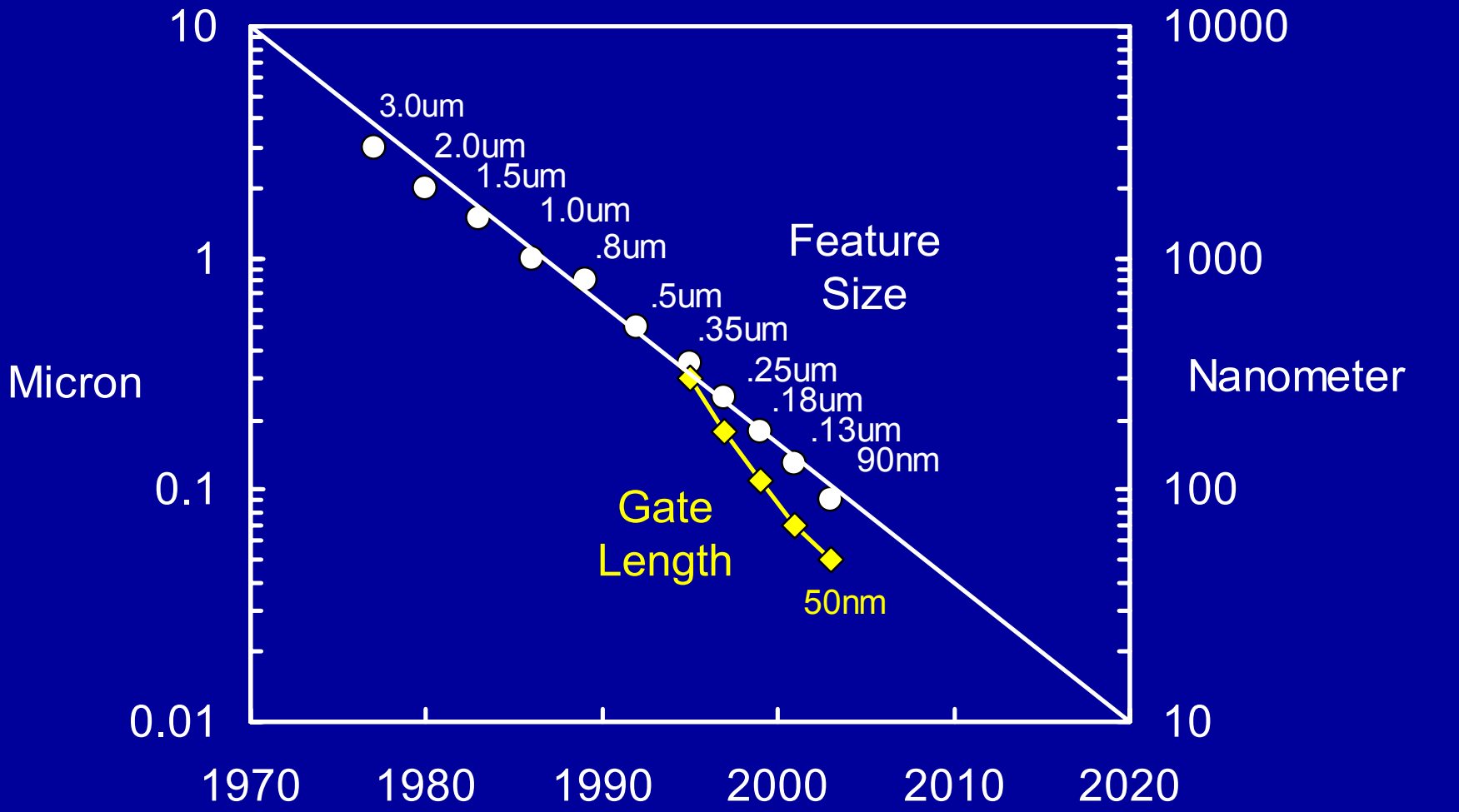
Feature Size Trend



Transistor gate length scaling faster for improved performance

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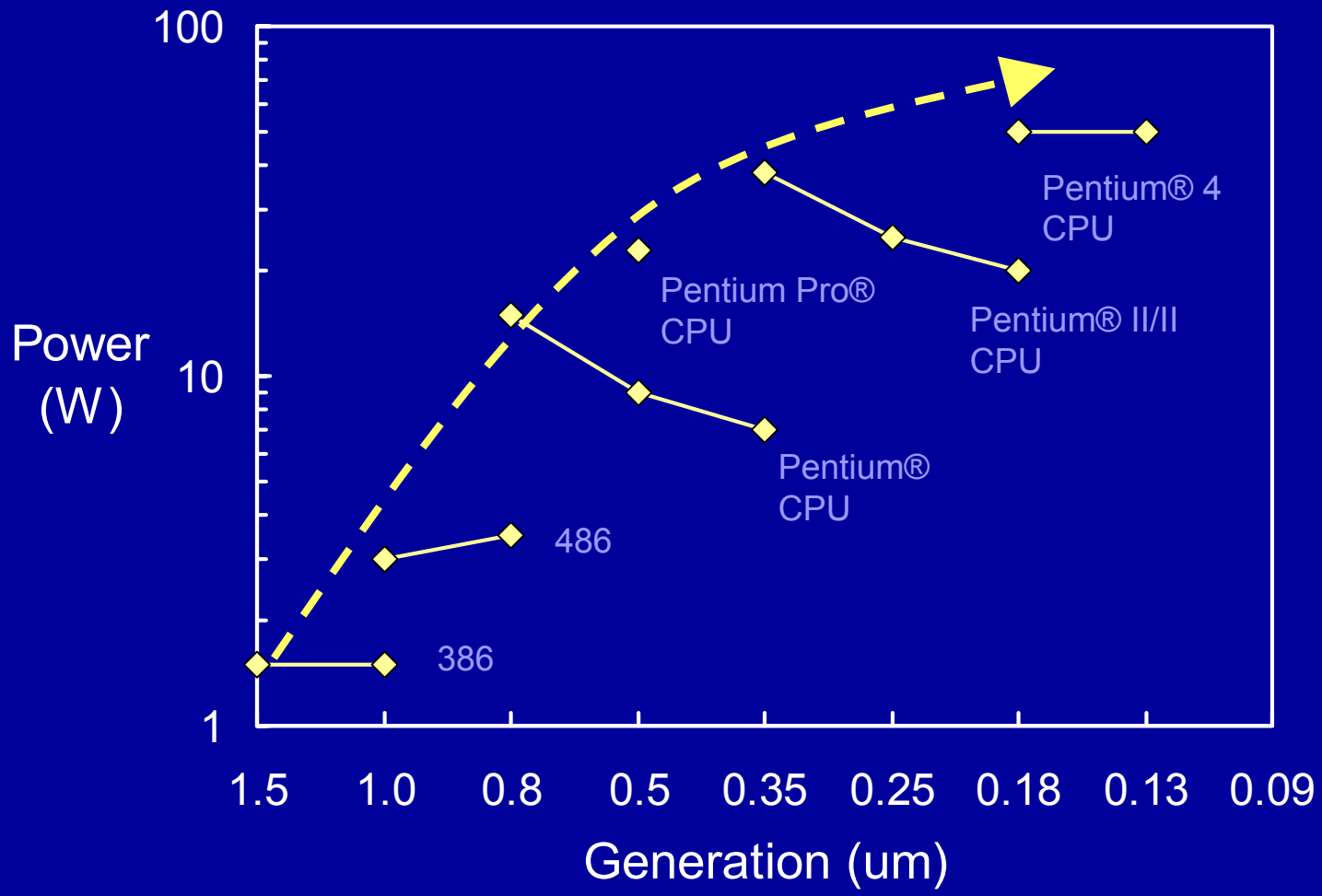
CPU Power Trend



CPU power growing due to increased operating frequency and increased transistor count

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Logic Technology Evolution

Each new technology generation provides:

- ~ 0.7x minimum feature size scaling
- ~ 2.0x increase in transistor density
- ~ 1.5x faster transistor switching speed
- Reduced chip power
- Reduced chip cost

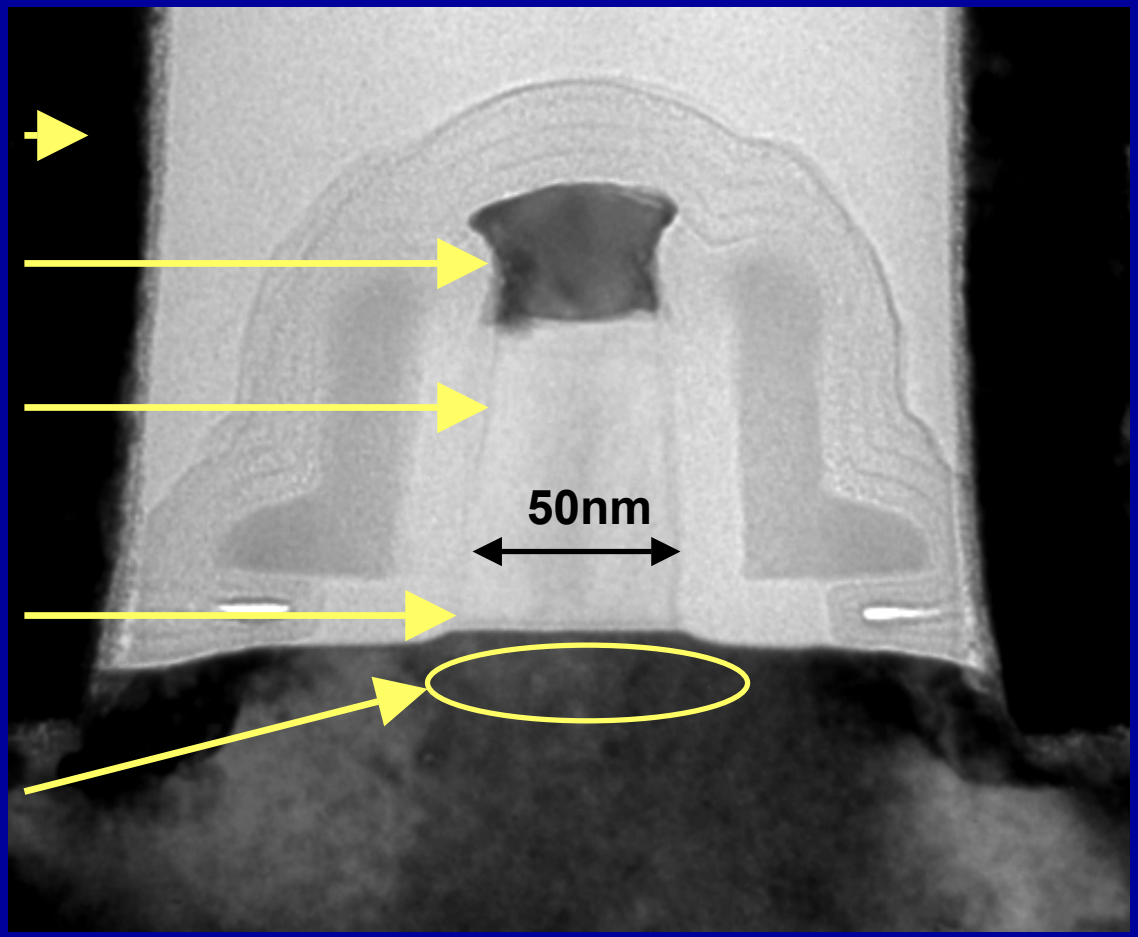
Outline

- Logic Technology Evolution
- 90 nm Logic Technology
- Future Scaling Challenges

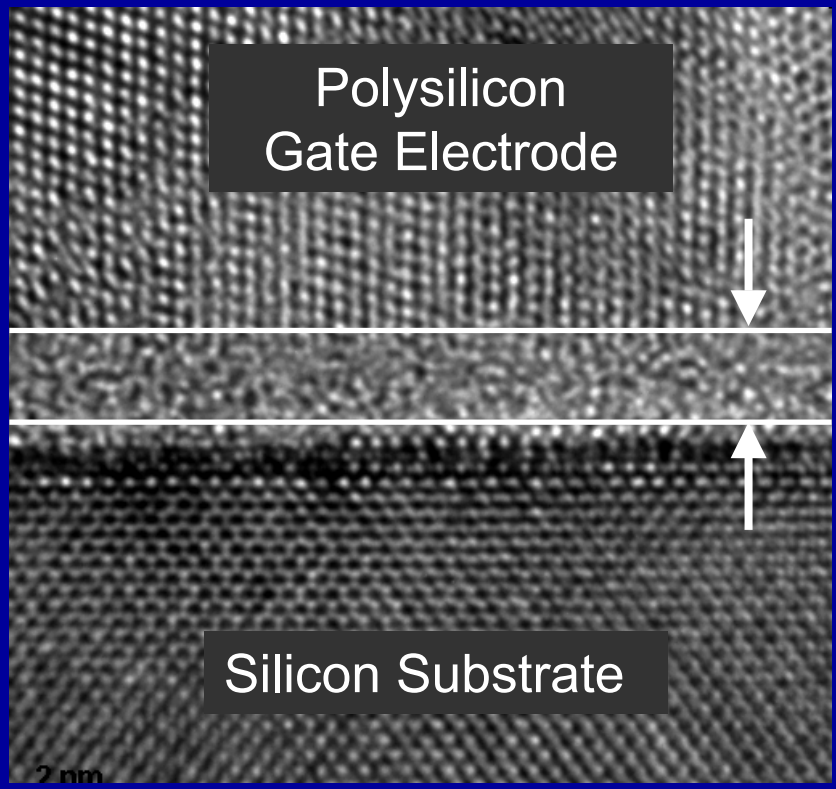
Key 90 nm Process Features

- High Speed, Low Power Transistors
  - 1.2 nm gate oxide
  - 50 nm gate length
  - Strained silicon technology
- Faster, Denser Interconnects
  - 7 copper layers
  - New low-k dielectric
- Lower Chip Cost
  - 1.0 μm^2 SRAM memory cell size
  - 300 mm wafers

90 nm Generation Transistor



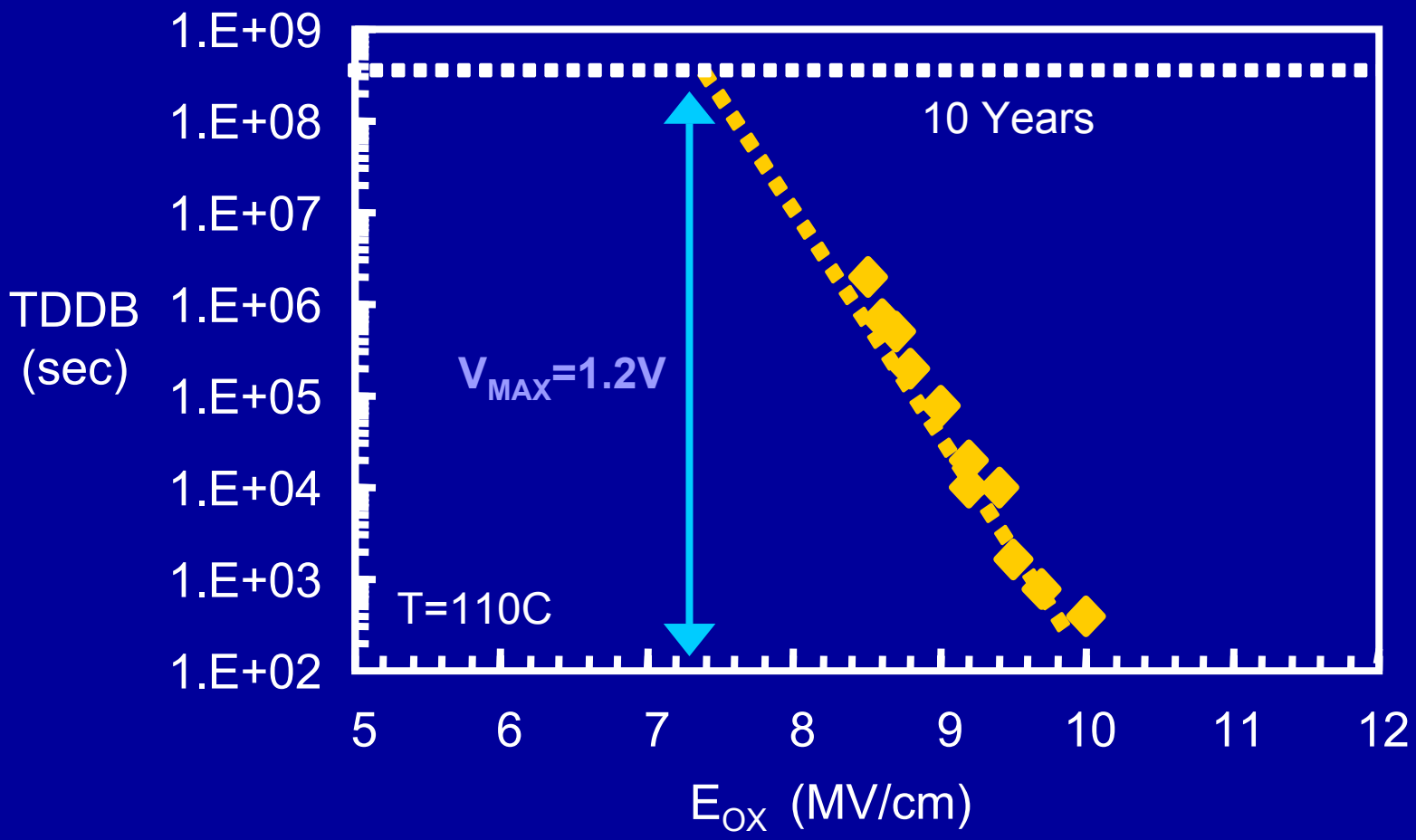
90 nm Generation Gate Oxide



1.2 nm SiO_2

Gate oxide is less than 5 atomic layers thick

1.2 nm Gate Oxide Reliability



1.2 nm gate oxide exceeds 1.2 V reliability criteria

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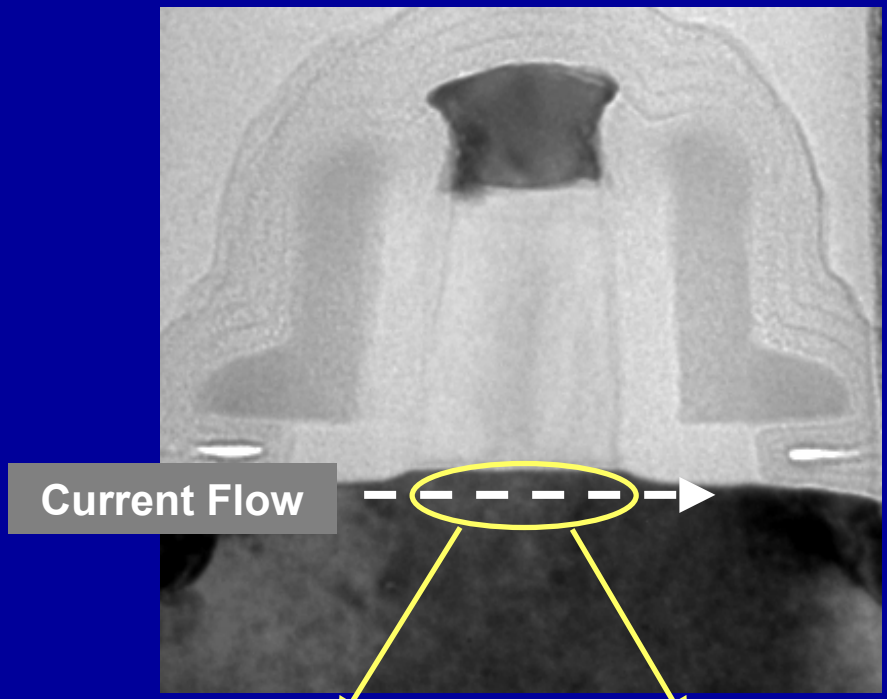
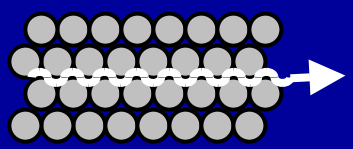
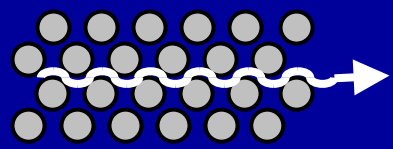
Strained Silicon Transistors



Normal electron flow



Normal Silicon Lattice



Faster electron flow

Strained Silicon Lattice

10-20% drive current increase

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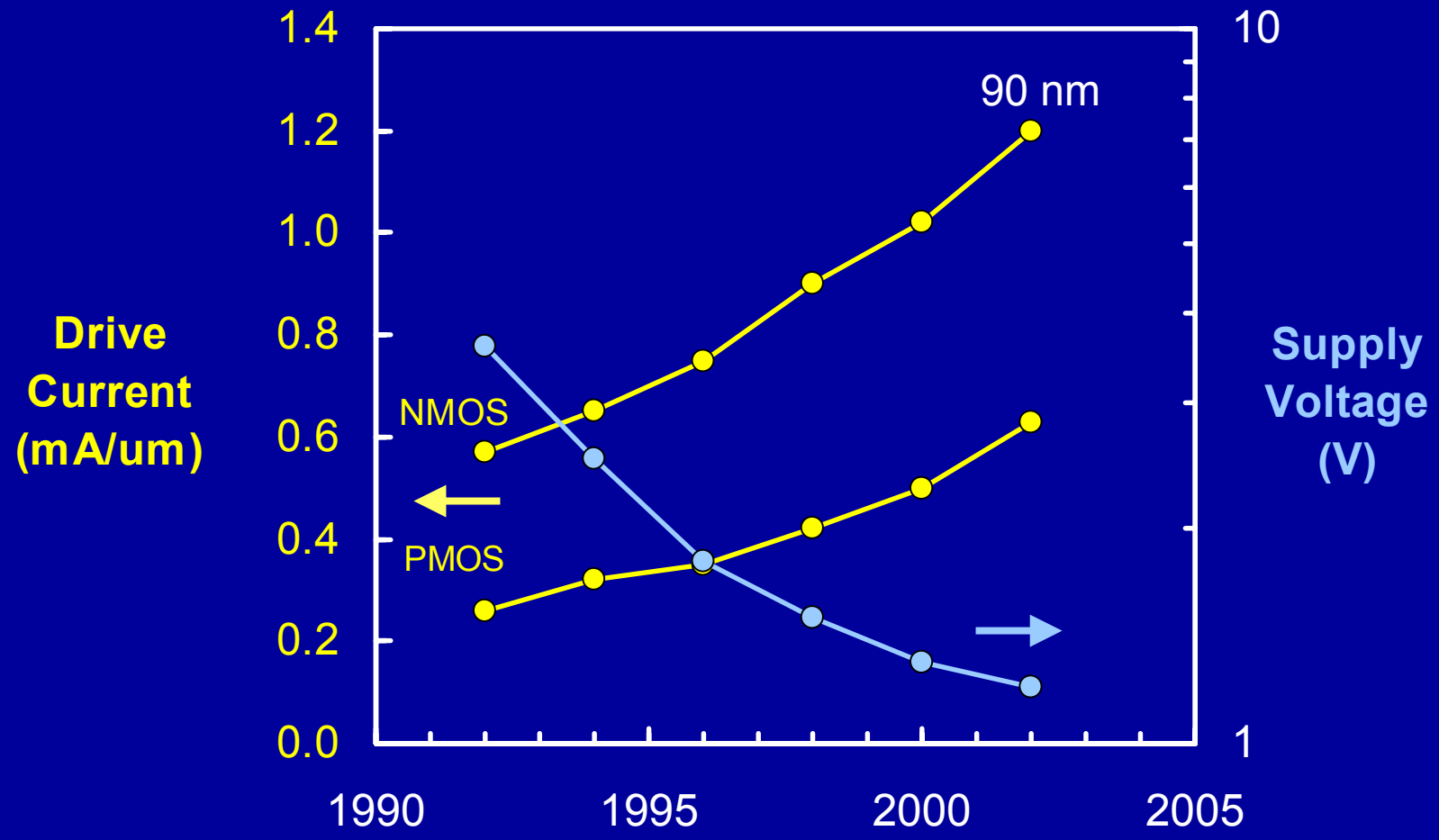
Transistor Performance Trend



- Increased drive current for performance
- Reduced voltage for power and reliability

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90 nm Generation Interconnects

7 layers of copper interconnect

- 1 more layer than 0.13 μm generation
- Extra layer provides cost effective improvement in logic density

New low-k dielectric introduced to reduce wire-wire capacitance

- Carbon-doped oxide (CDO) dielectric reduces capacitance by 18% compared to SiOF dielectric used on 0.13 μm
- Reduced capacitance speeds up intra-chip communication and reduces chip power

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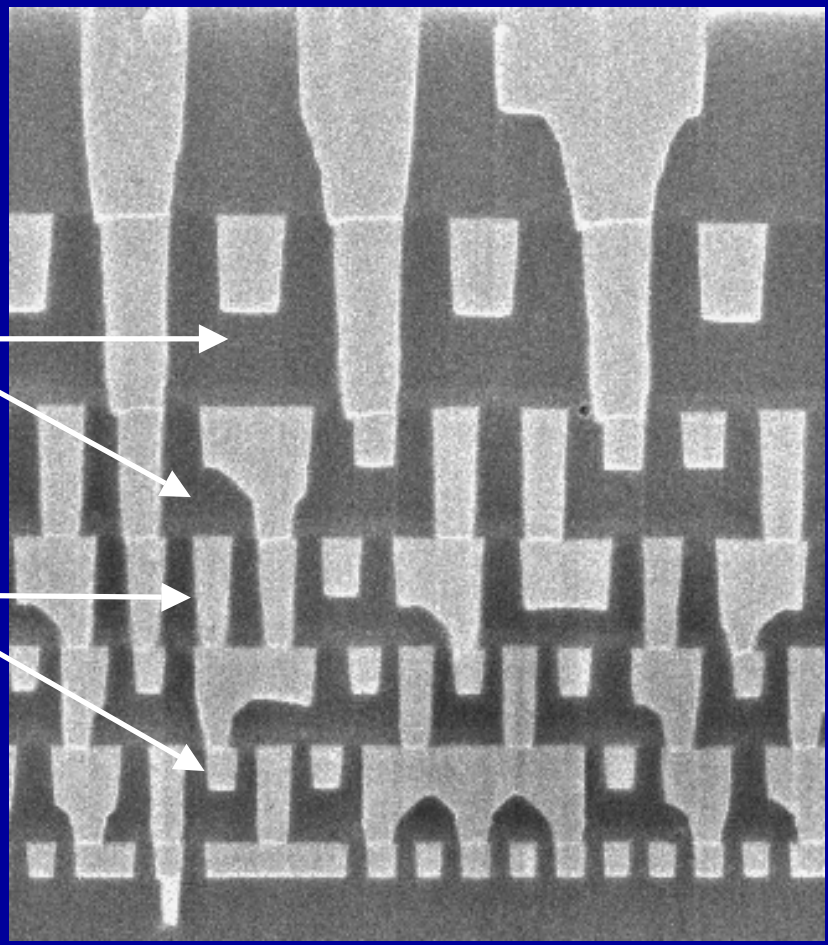
90 nm Generation Interconnects



	pitch
M7	1080 nm
M6	720 nm
M5	480 nm
M4	400 nm
M3	320 nm
M2	320 nm
M1	220 nm

Coarse pitch at upper layers for low resistance
Fine pitch at lower layers for high density

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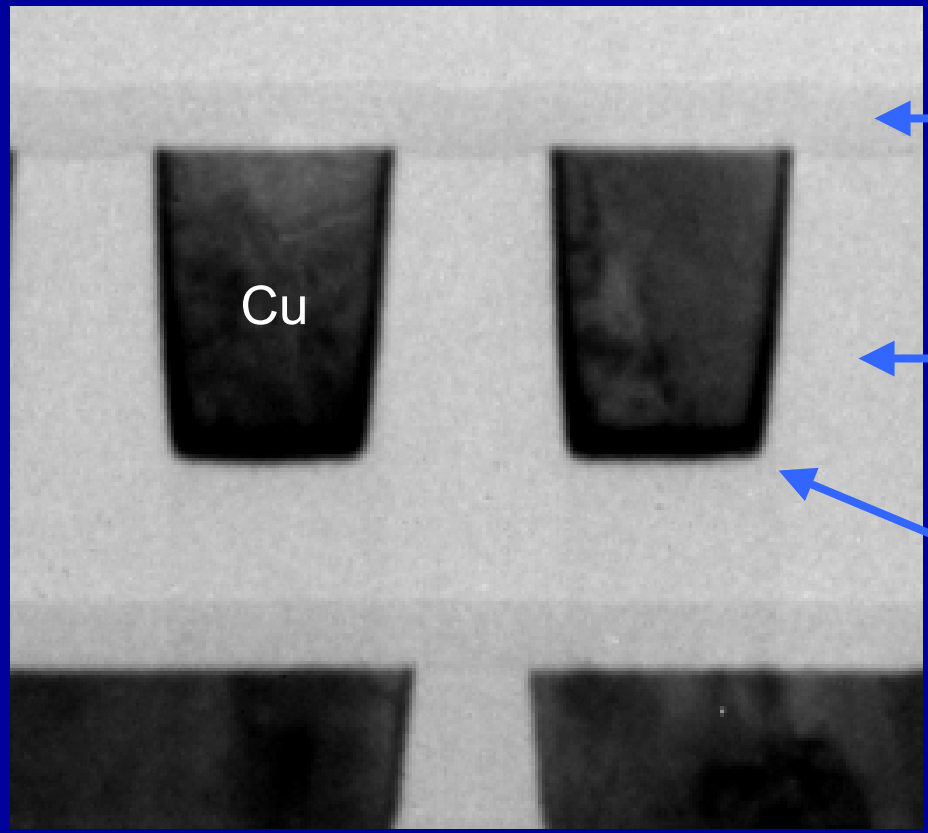
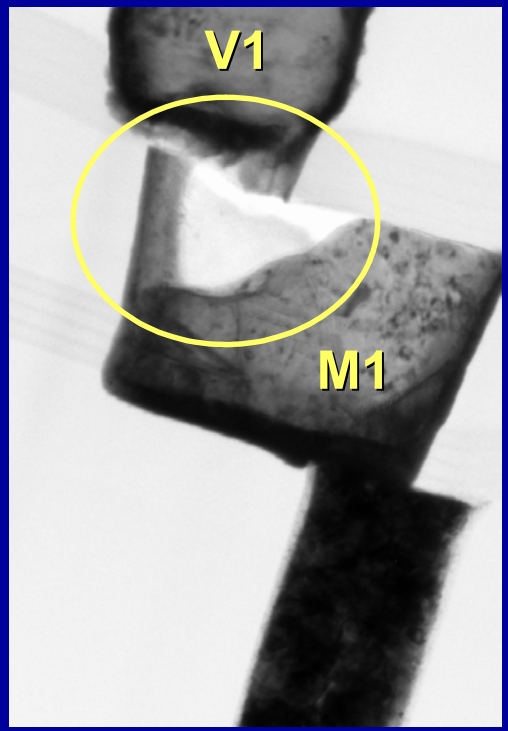
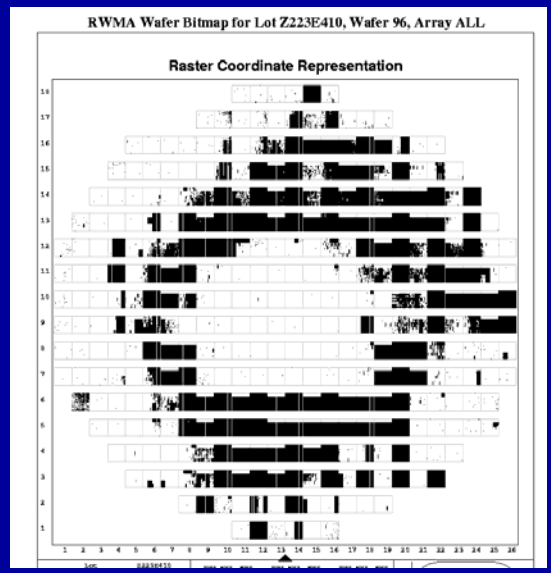
Cu + CDO Interconnects



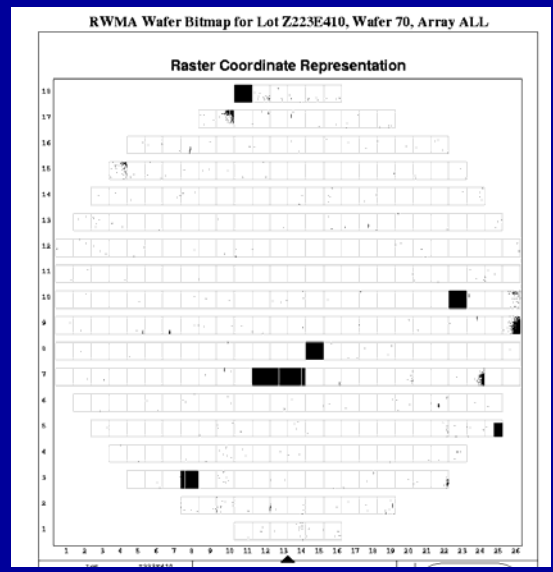
Void-Free Required for Electromigration



Old Process

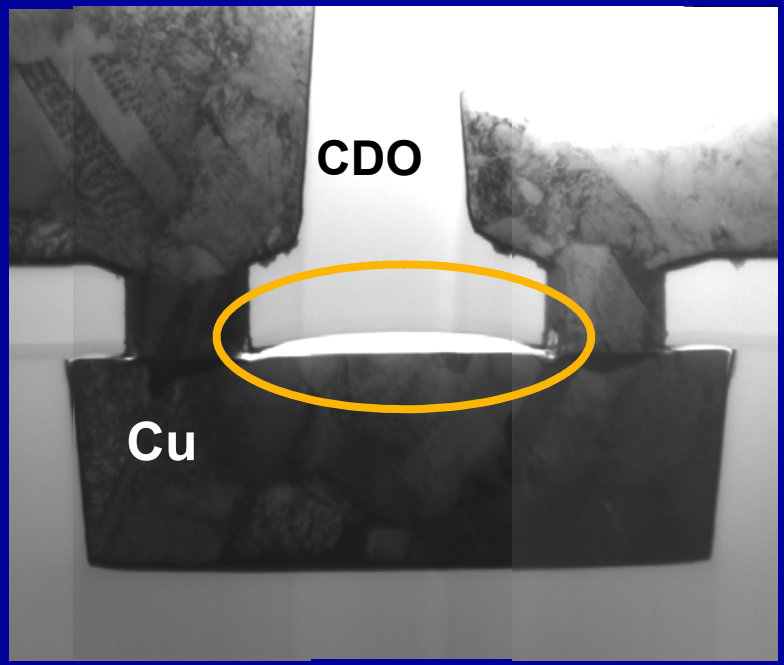


New Process

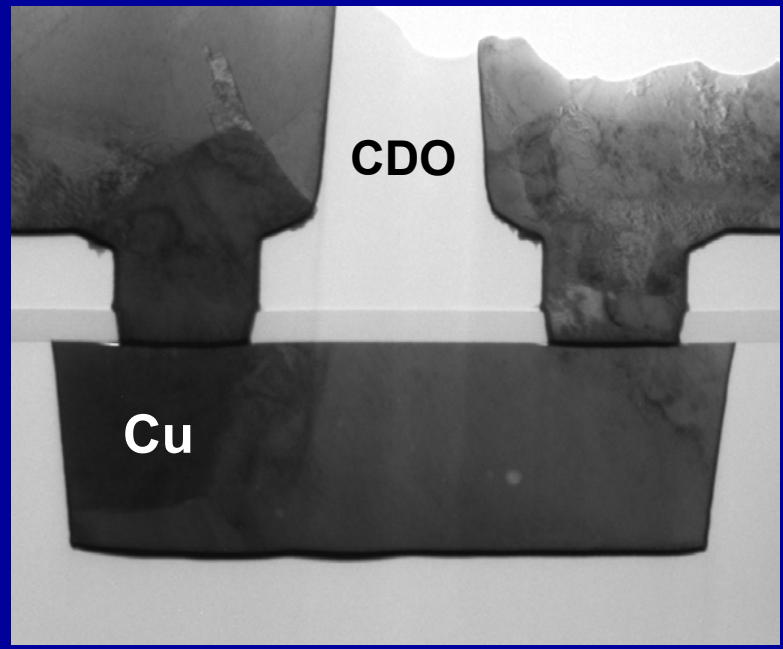


Electromigration Enabling

Old process



New process



Interface controls EM performance

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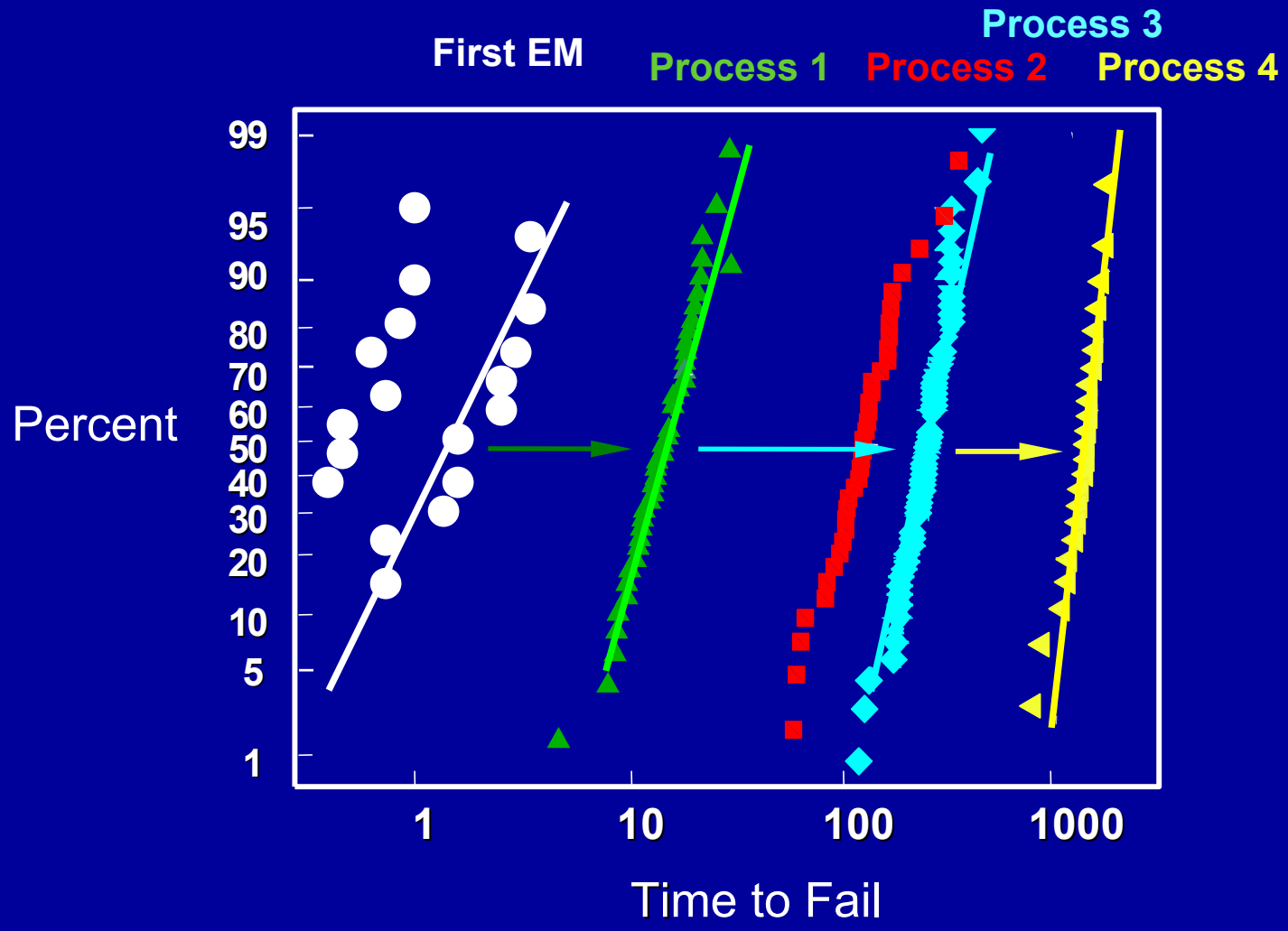
Electromigration Improvement



6-T SRAM Cell

- SRAM cell has area of 1.0 μm^2
- Same process as high performance logic
- Small memory cell enables cost effective increase in CPU performance by adding more on-die cache memory

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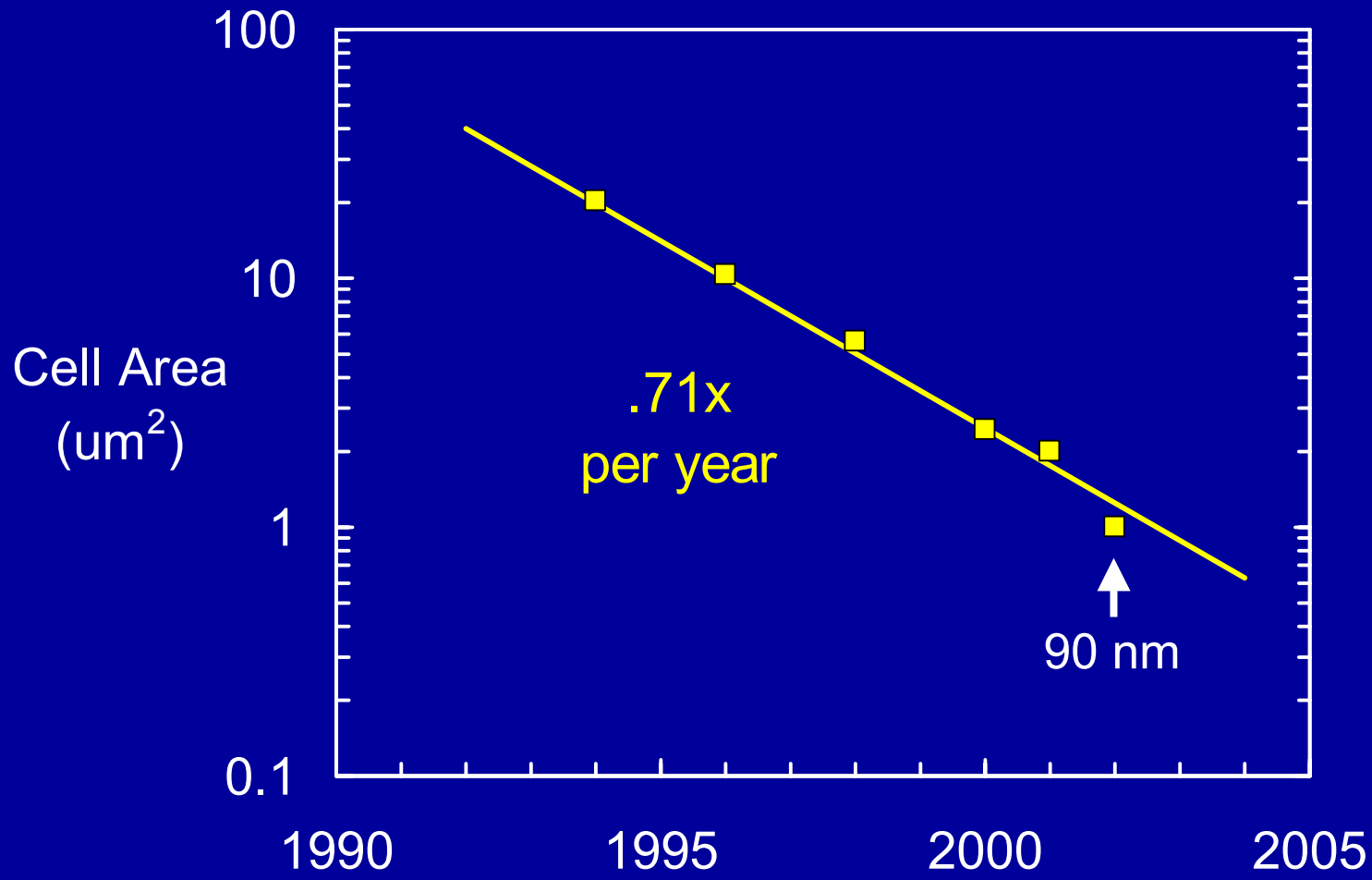
Intel SRAM Cell Size Trend

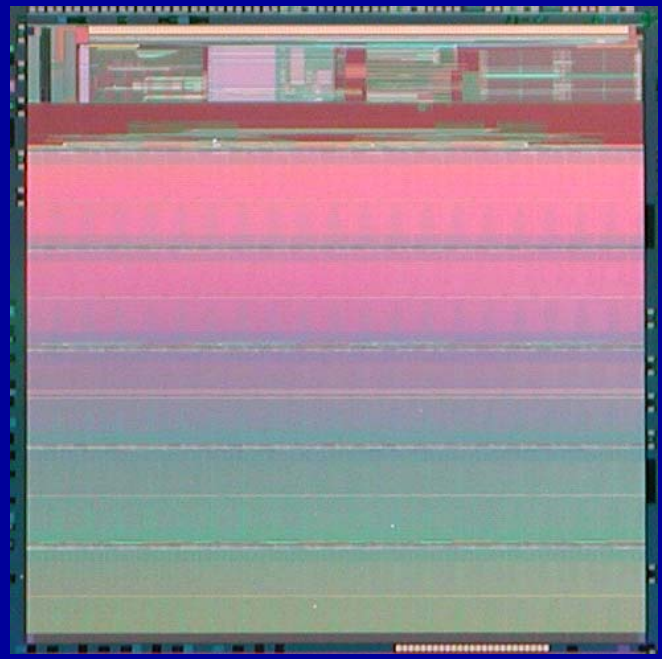


90 nm cell is ~half the area of 130 nm generation cell

52 Mbit SRAM on 90 nm Process

10.1 mm

10.8 mm



330 million transistors on single chip

Initial 90 nm process certification vehicle

Same process and design rules as CPU products

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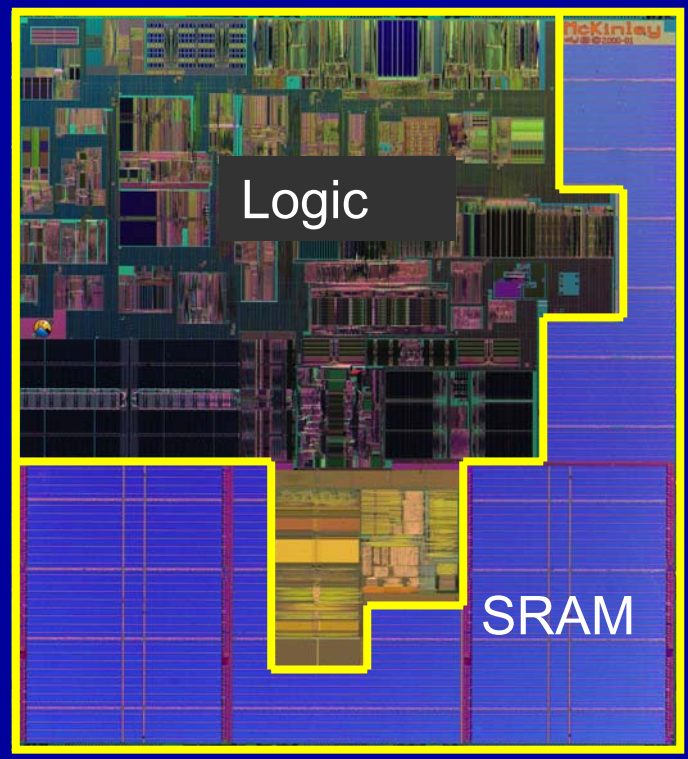
Same Process for Logic and SRAM

- Microprocessors use same transistors and interconnects for Logic and SRAM
- On-die SRAM cache transistor count increasing for improved performance



0.18 µm Itanium® 2 Processor
144M SRAM, 220M Total

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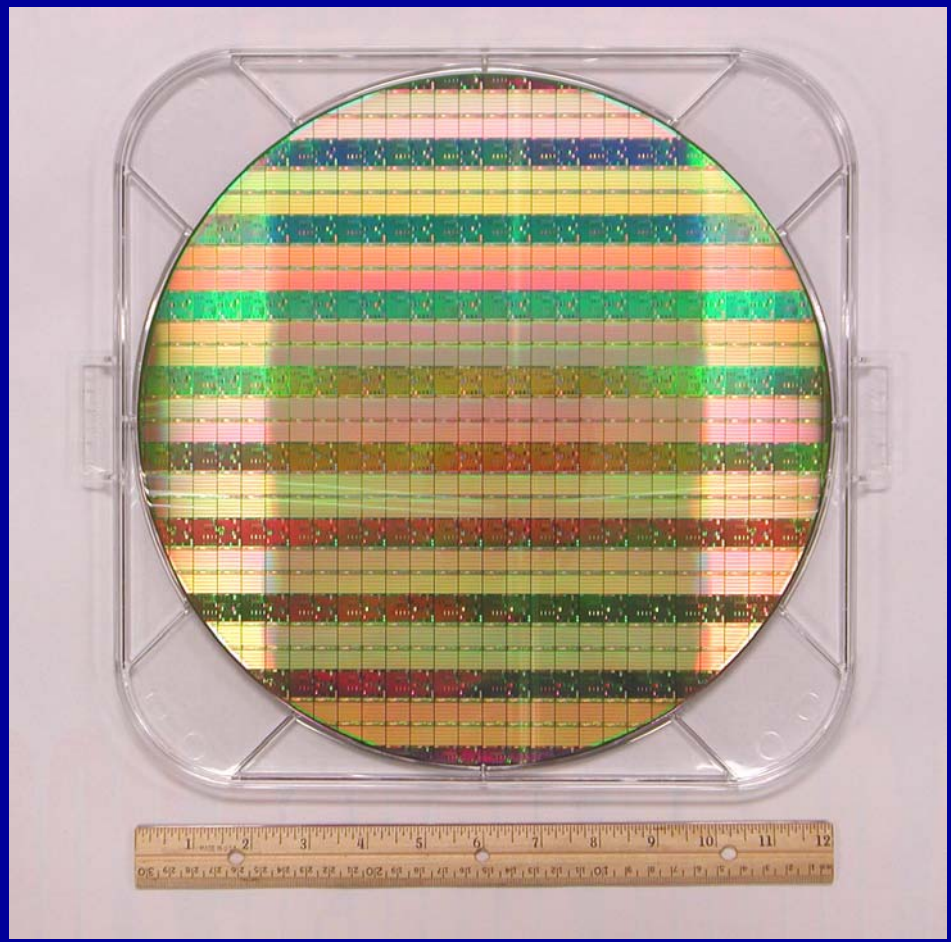
52 Mbit SRAM Chips on 300 mm Wafer



120 billion transistors on one wafer

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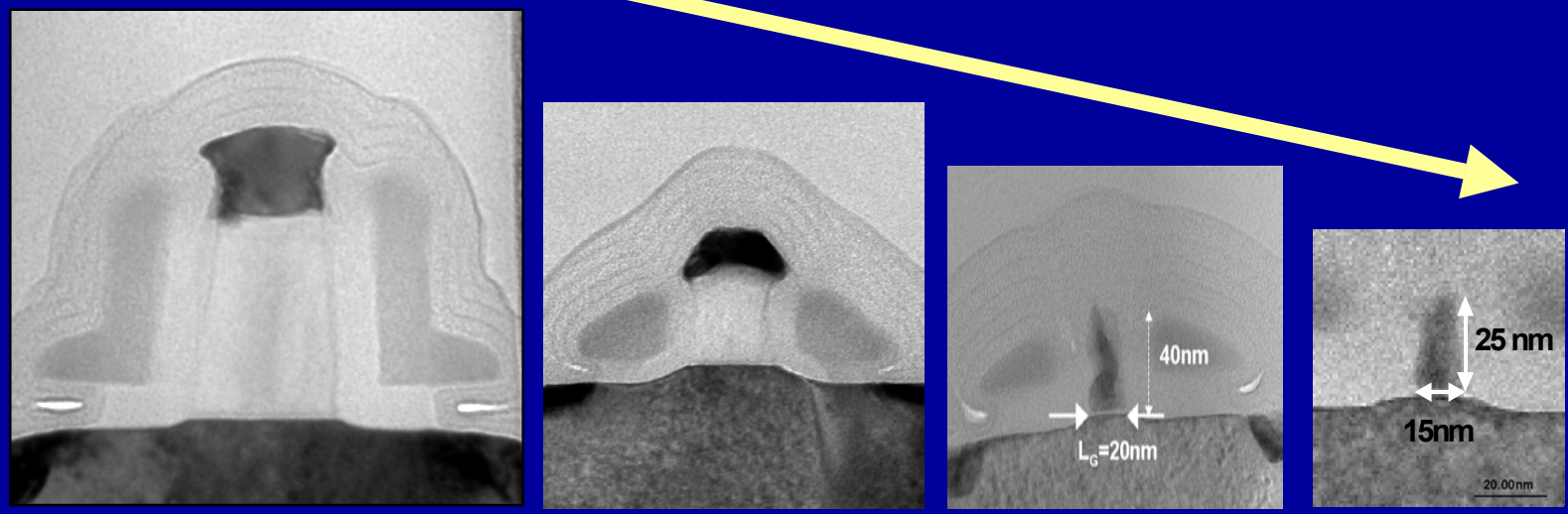
Outline

- Logic Technology Evolution
- 90 nm Logic Technology
- Future Scaling Challenges

Planar CMOS Transistor Scaling

Today

Future



50 nm 30 nm 20 nm 15 nm

Gate Length

R&D groups exploring aggressive scaling
of conventional planar CMOS transistors

Source: Intel Components Research

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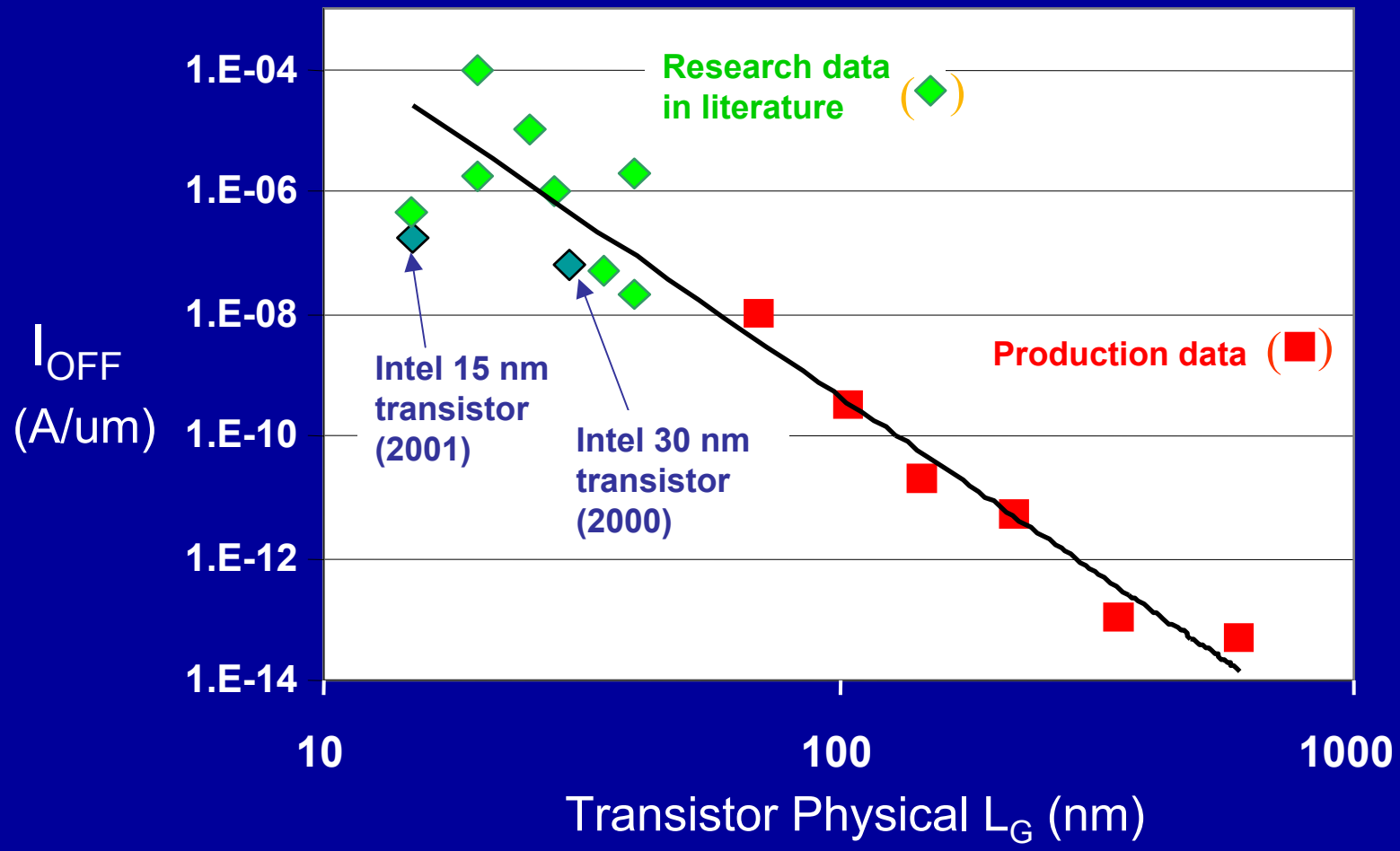
Transistor I_{OFF} Leakage Trend



- Transistor leakage current increasing as V_T scales
- Leakage power is becoming a larger % of total chip power

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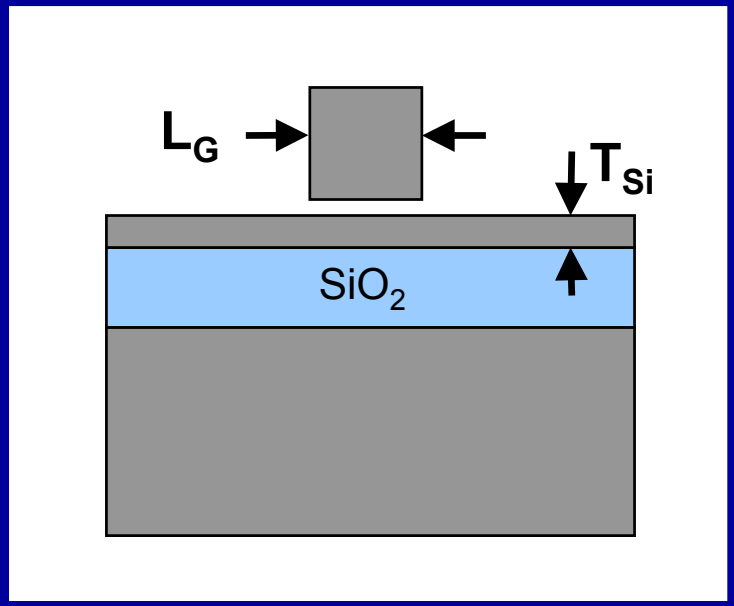
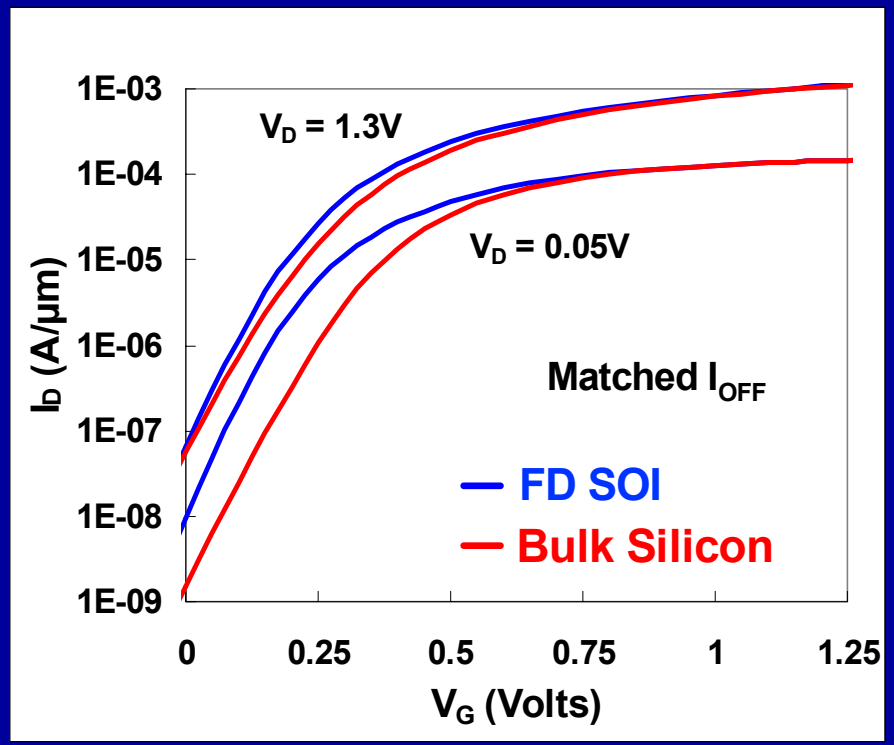
Fully Depleted Transistors



Fully-Depleted SOI (planar)



Source: Intel Components Research

- FD SOI provides steeper sub-threshold slope, which can be used to reduce I_{OFF} or increase I_{DSAT}
- Cost and controllability of thin SOI layer are key manufacturing problems

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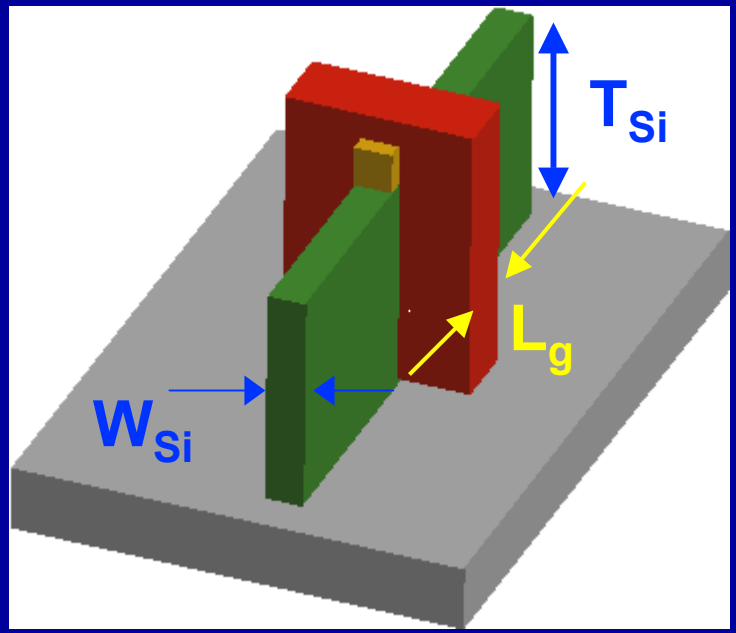
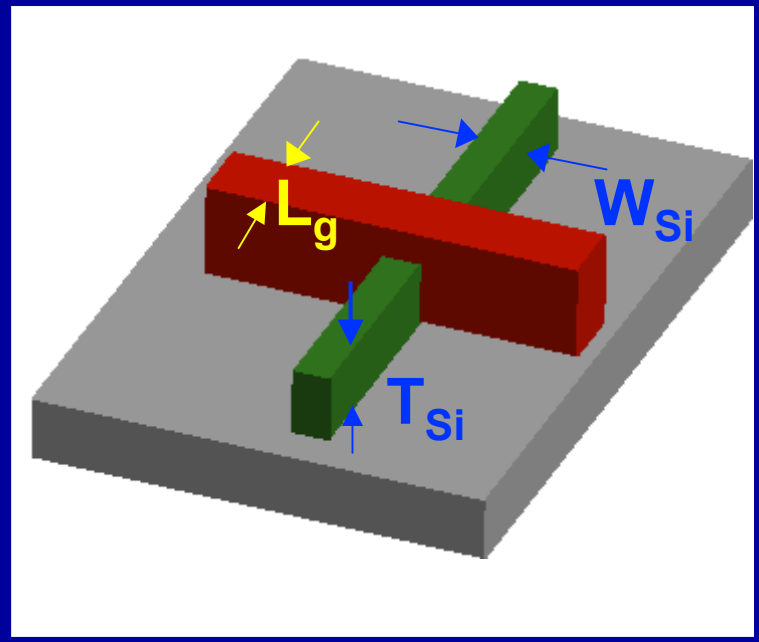
Fully Depleted Transistors



Double-Gate (non-planar)



Tri-Gate (non-planar)

Double-gate or triple-gate devices offer steep sub-threshold slope, but with more complex process than planar transistors

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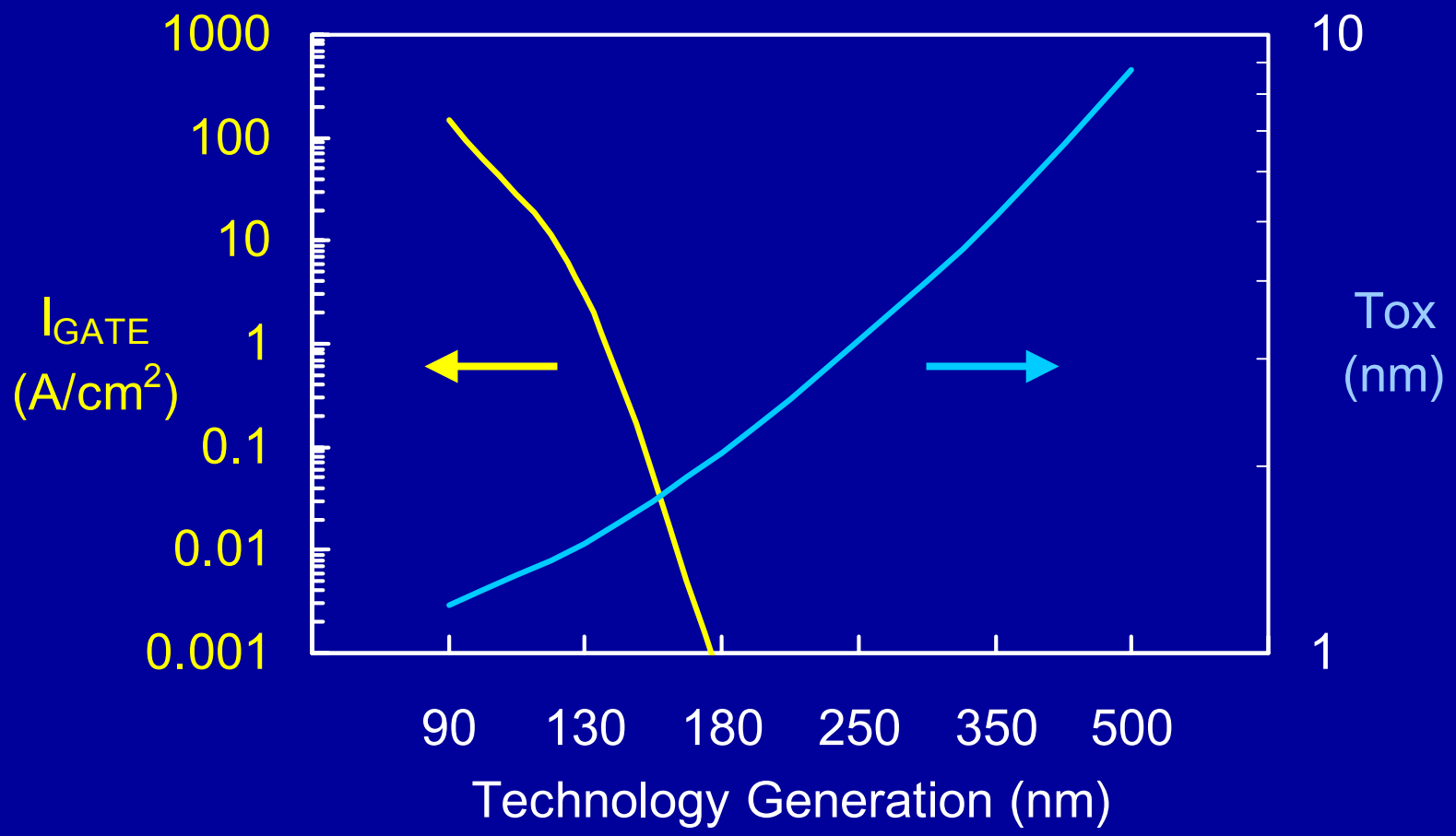
Transistor I_{GATE} Leakage Trend



Gate oxide leakage increasing exponentially due to tunneling current

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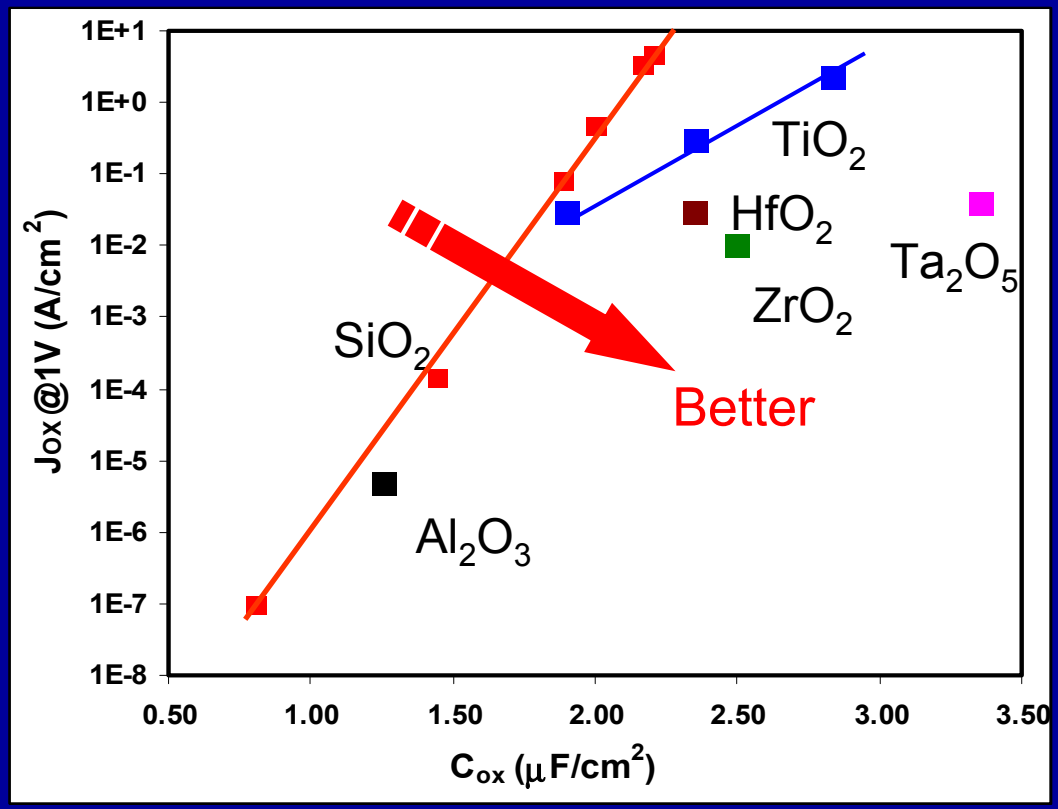
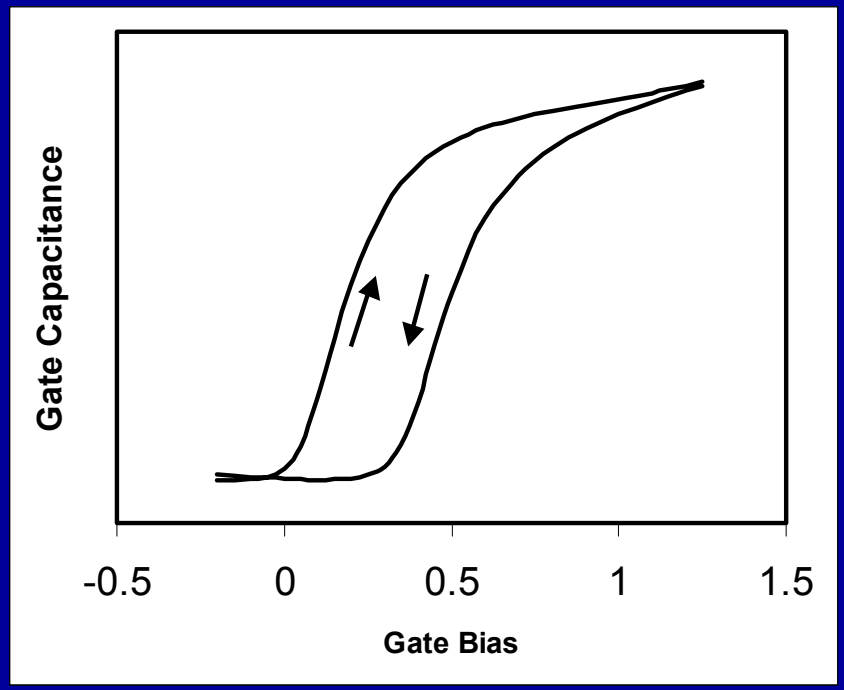
High-k Gate Dielectric



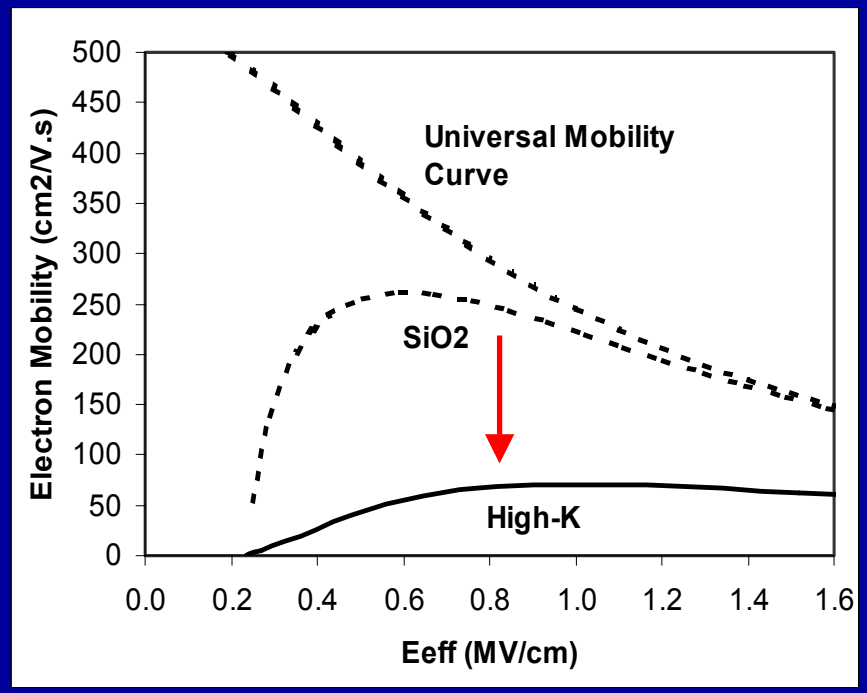
Source: Intel Components Research

High-k dielectrics provide higher capacitance and reduced leakage

Early Problems with High-K Dielectrics



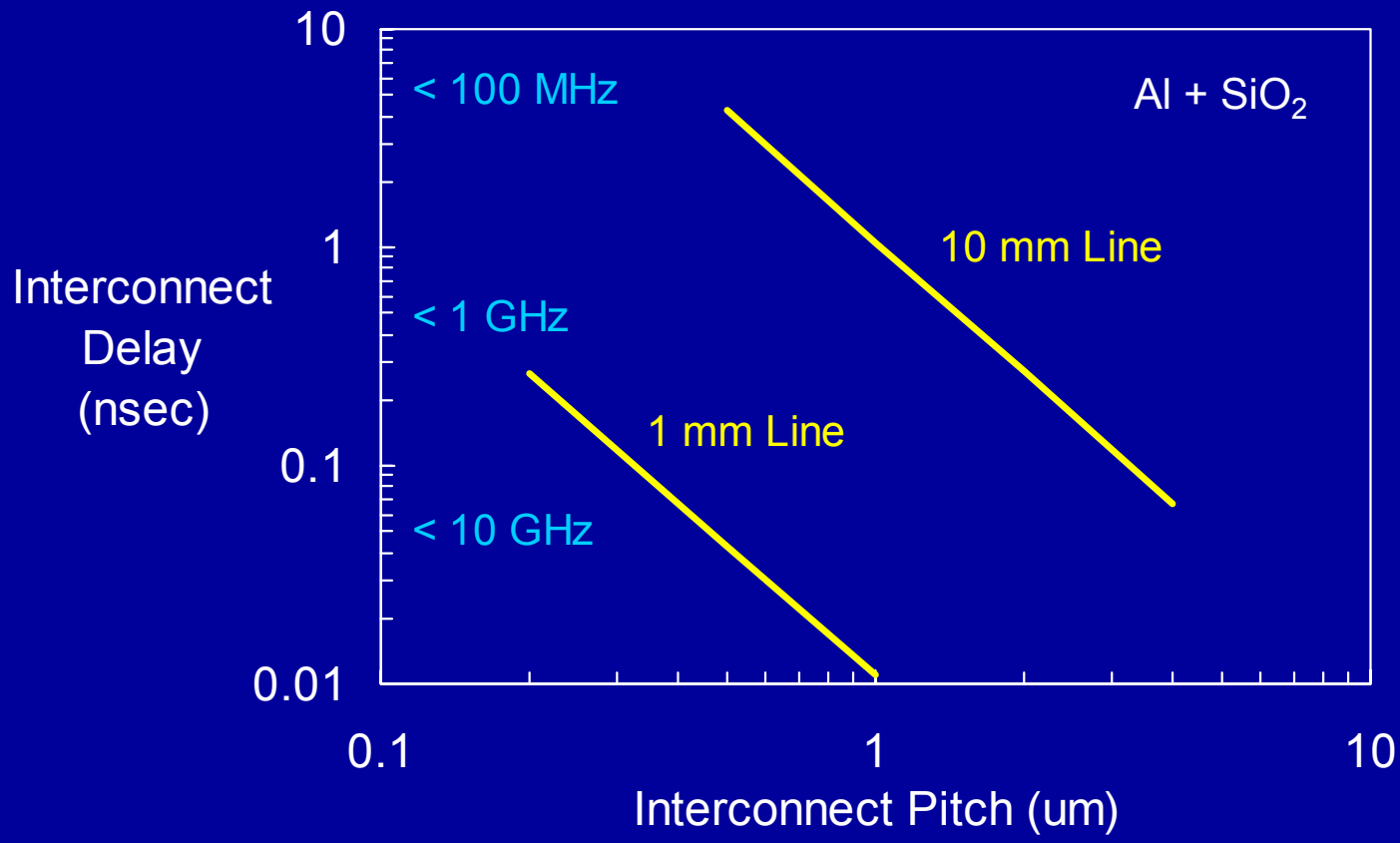
V_T instability due to charge traps



Degraded inversion layer mobility

SiO_2 will be difficult to replace as the gate dielectric

Interconnect Delay



- Interconnect delay getting worse as pitch scales
- Scaling line length helps keep delay constant
- Material changes such as Cu and low-k needed for lower RC
- Adding more metal layers is an expensive alternative

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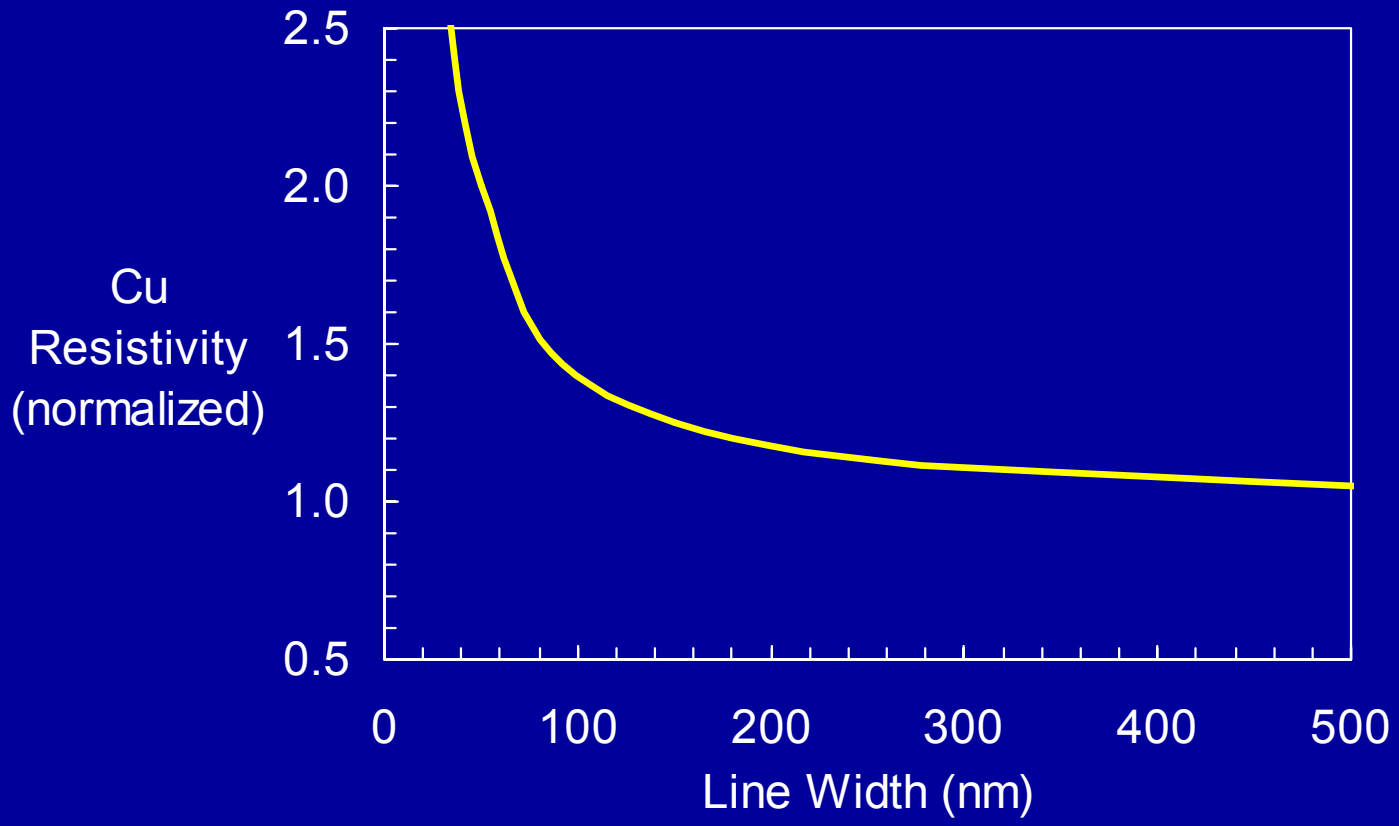
Narrow Line Width Resistivity Increase



Cu resistivity increases for narrow lines due to:

- Finite barrier layer thickness
- Electron mean free path comparable to line width

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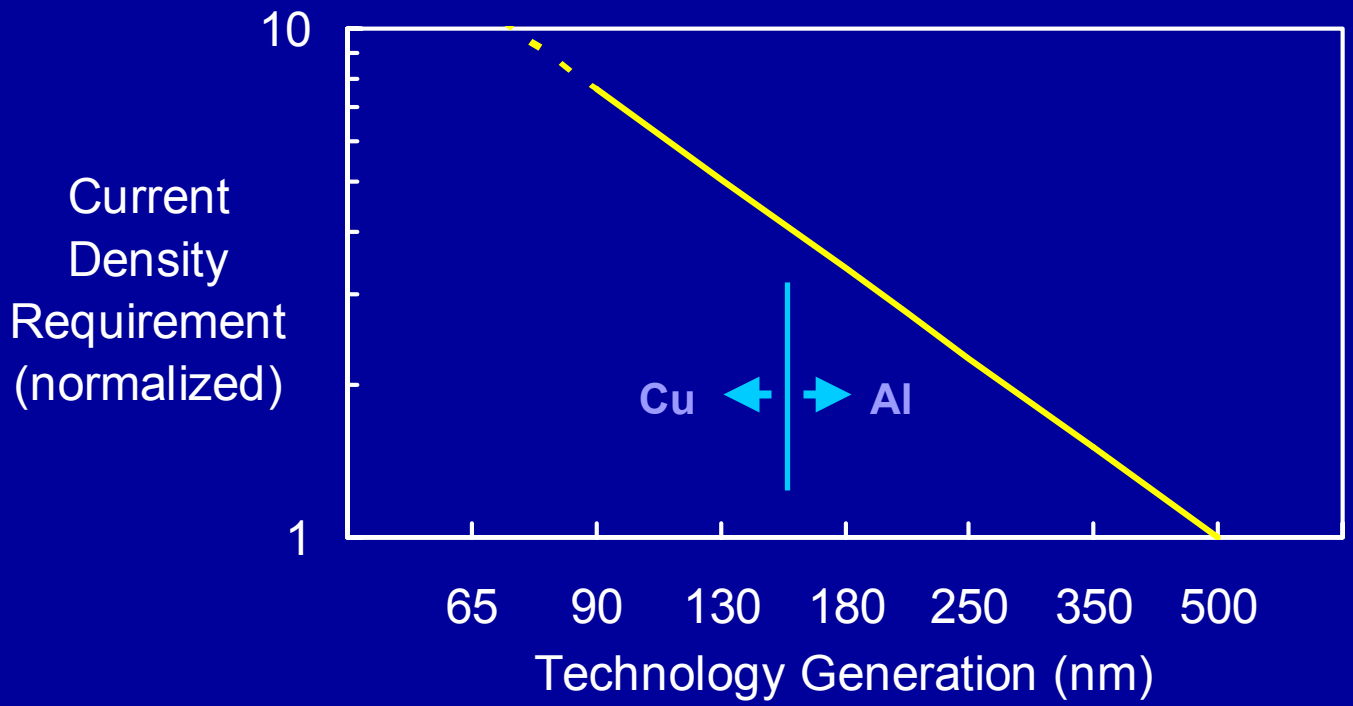
Electromigration Requirements



- Current density increases ~1.5x per generation as feature size decreases and operating frequency increases
- EM improved on Al by adding alloy ingredients and shunt layers
- Change to Cu provided big EM boost, but future generations will need Cu EM improvements

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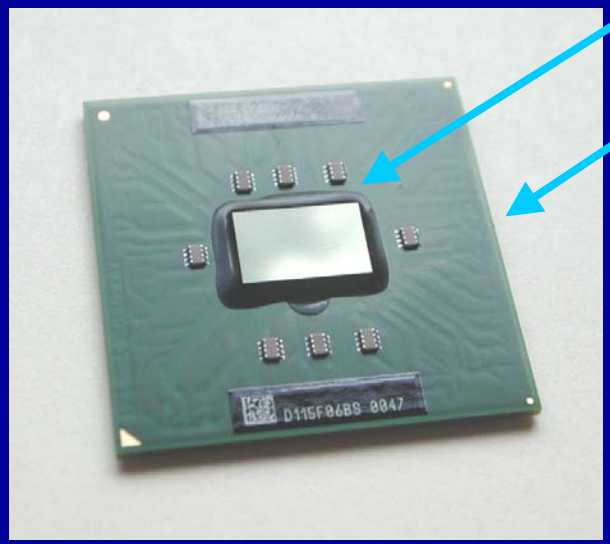
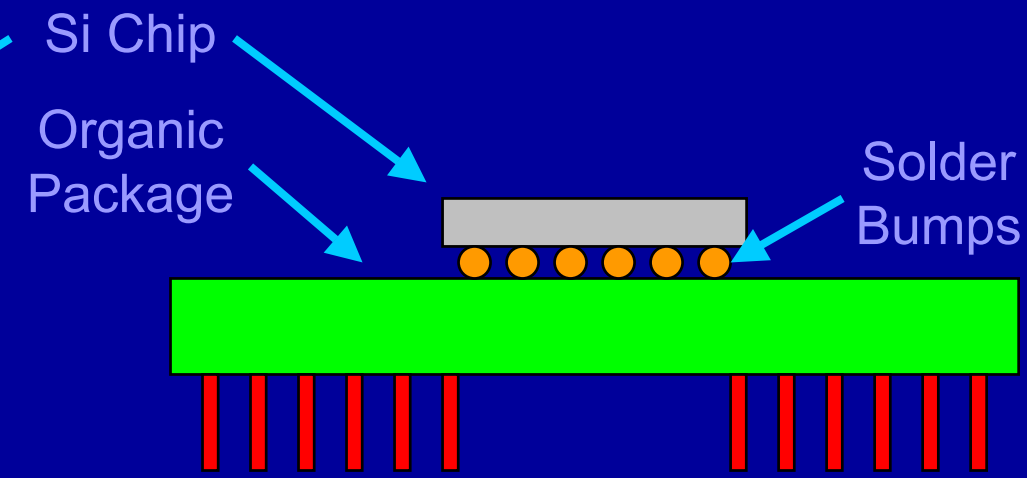
Fragile Low-k Dielectric Materials





- Low-k dielectric materials are mechanically weaker than SiO_2
- CTE mismatch between chip and package causes stress during chip bonding step
- Stress can cause interconnect deformation or ILD cracking

Summary

- High performance logic technology has scaled at a rapid pace down to the 90 nm generation, providing significant gains in density and performance
- Going forward, transistor and interconnect scaling challenges look formidable
- New materials and new device structures are needed and options are emerging that show promise for continued scaling

For further information on Intel's silicon technology, please visit:

www.intel.com/research/silicon